Claim(s)

What is claimed is:

1. A method for characterizing a circuit described by a logic model, wherein the circuit includes a plurality of registers wherein each register sets a state of a corresponding register output signal to match a state of a corresponding register input signal whenever clocked by a succession of clock signal edges, and wherein the circuit also includes circuit logic controlling the state of each register input signal in logical response to circuit input and register output signals, the method comprising the steps of:

a. processing the logic model to perform a simulation of circuit behavior thereby producing waveform data indicating states of circuit input and register output signals as functions of time;

b. processing the logic model to generate a plurality of net models, each net model corresponding to a separate one of the registers and depicting a logical relationship between the register's input signal and all others of the circuit input and register output signals that influence a state of the corresponding register's input signal between clock signal edges; and

c. generating a display including a plurality of register symbols, each register symbol indicating a state of a register output signal produced by a corresponding register after being clocked by a pulse signal edge as indicated by the waveform data, wherein the display also includes a representation of a logical relationship depicted by at least one of the net models.

2. The method in accordance with claim 1 wherein each register symbol is horizontally positioned in the display to represent timing of one of the clock signal edges.

3. The method in accordance with claim 1 wherein the representation of a logical relationship comprises data included in the display indicating that a state of a register

input signal of a register corresponding to one of the displayed register symbols is a logical function of a state of a register output signal of a register corresponding to at least one other of the displayed register symbols.

4. The method in accordance with claim 1 wherein the display also includes a plurality of circuit input signal symbols, each input signal symbol depicting a state of a circuit input signal at a separate time during the simulation.

5. The method in accordance with claim 4 wherein each input signal symbol is horizontally positioned in the display to represent a time at which the input signal is of the depicted state.

6. The method in accordance with claim 4 wherein the representation of a logical relationship comprises data included in the display indicating that a state of a register input signal of a register corresponding to one of the displayed register symbols is a logical function of a state of a register output signal of a register corresponding to at least one other of the displayed register symbols and of a state of an input signal depicted by one of the displayed input signal symbols.

7. The method in accordance with claim 1 wherein the representation of a logical relationship comprises a line interconnecting two of the register symbols.

8. The method in accordance with claim 1 wherein the representation of a logical relationship comprises a graphical representation of one of the net models linking two of the registers.

9. The method in accordance with claim 4 wherein the representation of a logical relationship comprises a first line interconnecting a first one of the register symbols to

a second one of the register symbols and a second line interconnecting the first one of the register symbols to one of the input signal symbols.

10. The method in accordance with claim 4 wherein the representation of a logical relationship comprises a graphical representation of one of the net models, wherein the graphic representation indicates how an input signal state depicted by one of the input signal symbols logically influences a state of a register input signal to a register corresponding to one displayed register symbol.

11. The method in accordance with claim 10

wherein each register symbol is horizontally positioned in the display to represent timing of one of the clock signal edges, and

wherein each input signal symbol is horizontally positioned in the display to represent the time at which the input signal is of the depicted state.

12. A method for characterizing a circuit including a plurality of registers and other logic, wherein each register sets a state of a corresponding register output signal to match a state of a corresponding register input signal whenever clocked by a succession of clock signal edges, and wherein the other logic controls the state of each register input signal in logical response to circuit input and register output signals, the method comprising the steps of:

a. displaying a plurality of register symbols, each register symbol indicating a state of a register output signal produced by a corresponding register after being clocked by a pulse signal edge as indicated by the waveform data, wherein a horizontal position of each register symbol represents a time of occurrence of a pulse signal edge;

b. displaying a plurality of input signal symbols, each indicating a state of the input signal at a separate time indicated by a horizontal position of the input signal system;

c. displaying a representation of logic interconnecting the register symbols and the input signal symbols indicating how indicated states of input signals and register output signals influence states of register input signals.

13. An apparatus for characterizing a circuit described by a logic model, wherein the circuit includes a plurality of registers wherein each register sets a state of a corresponding register output signal to match a state of a corresponding register input signal whenever clocked by a succession of clock signal edges, and wherein the circuit also includes circuit logic controlling the state of each register input signal in logical response to circuit input and register output signals, the apparatus comprising:

a logic synthesizer for processing the logic model to perform a simulation of circuit behavior thereby producing waveform data indicating states of circuit input and register output signals as functions of time;

means for processing the logic model to generate a plurality of net models, each net model corresponding to a separate one of the registers and depicting a logical relationship between the register's input signal and all others of the circuit input and register output signals that influence a state of the corresponding register's input signal between clock signal edges; and

c. means for generating a display including a plurality of register symbols, each register symbol indicating a state of a register output signal produced by a corresponding register after being clocked by a pulse signal edge as indicated by the waveform data, wherein the display also includes a representation of a logical relationship depicted by at least one of the net models.

14. The apparatus in accordance with claim 13 wherein each register symbol is horizontally positioned in the display to represent timing of one of the clock signal edges.

15. The apparatus in accordance with claim 13 wherein the representation of a logical relationship comprises data included in the display indicating that a state of a register input signal of a register corresponding to one of the displayed register symbols is a logical function of a state of a register output signal of a register corresponding to at least one other of the displayed register symbols.

16. The apparatus in accordance with claim 14 wherein the display also includes a plurality of circuit input signal symbols, each input signal symbol depicting a state of a circuit input signal at a separate time during the simulation.

17. The apparatus in accordance with claim 16 wherein each input signal symbol is horizontally positioned in the display to represent time at which the input signal is of the depicted state.

18. The apparatus in accordance with claim 16 wherein the representation of a logical relationship comprises data included in the display indicating that a state of a register input signal of a register corresponding to one of the displayed register symbols is a logical function of a state of a register output signal of a register corresponding to at least one other of the displayed register symbols and of a state of an input signal depicted by one of the displayed input signal symbols.

19. The apparatus in accordance with claim 13 wherein the representation of a logical relationship comprises a line interconnecting two of the register symbols.

20. The apparatus in accordance with claim 13 wherein the representation of a logical relationship comprises a graphical representation of one of the net models linking two of the registers.

21. The apparatus in accordance with claim 17 wherein the representation of a logical relationship comprises a first line interconnecting a first one of register symbols to a second one of the register symbols and a second line interconnecting the first one of the register symbols to one of the input signal symbols.

22. The apparatus in accordance with claim 17 wherein the representation of a logical relationship comprises a graphical representation of one of the net models, wherein the graphic representation indicates how an input signal state depicted by one of the input signal symbols logically influences a state of a register input signal to a register corresponding to one displayed register symbol.

23. The apparatus in accordance with claim 22

wherein each register symbol is horizontally positioned in the display to represent timing of one of the clock signal edges, and

wherein each input signal symbol is horizontally positioned in the display to represent a time at which the input signal is of the depicted state.

24. An apparatus for characterizing a circuit described by a circuit logic model as having a set of clocked registers interconnected by un-clocked logic, the apparatus comprising:

a circuit simulator for processing the circuit logic model to produce waveform data indicating states of circuit input signals and of register output signals as functions of clock signal edge timing; and

means for processing the waveform data and the logic model to produce a temporal schema model characterizing the circuit's logic and behavior, and

means for producing a display based on the temporal schema model using separate symbols to represent successive circuit input signal states and successive register output signal states relative to various clock signal edges during the simulation behavior, wherein the display also graphically

depicts fan-in or fan-out logical relationships by which circuit input signal states and register output signal states influence register input signal states.